AX88772

USB to 10/100 Fast Ethernet/HomePNA Controller

Document No: AX88772_11/4/24/07

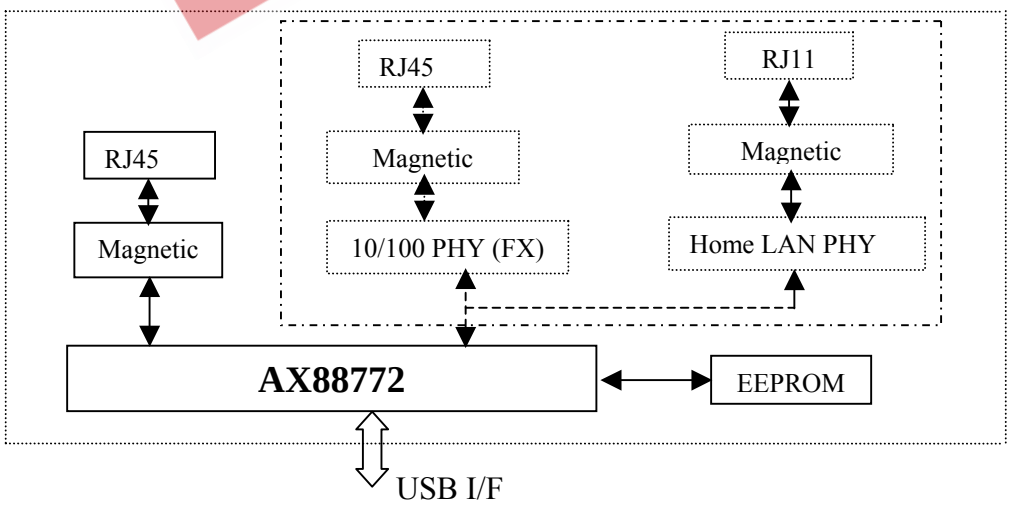
Features

- Single chip USB to 10/100 Fast Ethernet and HomePNA and HomePlug Network Controller
- Integrates on-chip 10/100Mbps Fast Ethernet PHY
- USB specification 1.1 and 2.0 compliant
- Supports USB Full and High Speed modes with Bus power capability
- Supports 4 endpoints on USB interface
- High performance packet transfer rate over USB bus using proprietary burst transfer mechanism (submitted for US patent application)
- IEEE 802.3 10BASE-T and 100BASE-TX compatible
- Embedded 20KB SRAM for RX packet buffering and 8KB SRAM for TX packet buffering
- Supports both full-duplex and half-duplex operation in Fast Ethernet
- Provides optional MII interface for Ethernet PHY and HomePNA/ HomePlug PHY interface
- Supports Suspend mode and Remote Wakeup via Link-up, Magic packet, or external pin
- Optional PHY power down during Suspend mode
- Supports 256/512 bytes (93c56/93c66) of serial EEPROM (for storing USB Descriptors)
- Supports automatic loading of Ethernet ID, USB Descriptors and Adapter Configuration from EEPROM after power-on initialization
- External PHY loop-back diagnostic capability
- Integrates on-chip 3.3V to 2.5V voltage regulator and requires only single power supply: 3.3V
- Small form factor with 128-pin LQFP package
- 12MHz and 25Mhz clock input from either crystal or oscillator source
- Operating temperature range: 0˚C to 70˚C.

Product Description

The AX88772 USB to 10/100 Fast Ethernet/HomePNA/HomePlug controller is a high performance and highly integrated ASIC with embedded 28KB SRAM for packet buffering. It enables low cost and affordable Fast Ethernet network connection to desktop, notebook PC, and embedded system using popular USB ports. It has an USB interface to communicate with USB host controller and is compliant with USB specification V1.1 and V2.0. It implements 10/100Mbps Ethernet LAN function based on IEEE802.3, and IEEE802.3u standards or HomePNA standard. It integrates an on-chip 10/100Mbps Ethernet PHY to simplify system design and provides an optional media-independent interface (MII) for implementing Fast Ethernet and HomePNA functions.

System Block Diagram



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Released Date: 4/24/2007

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1.0 Introduction

1.1 General Description

The AX88772 USB to 10/100 Fast Ethernet/HomePNA/HomePlug controller is a high performance and highly integrated ASIC with embedded 28KB SRAM for packet buffering. It enables low cost and affordable Fast Ethernet network connection to desktop, notebook PC, and embedded system using popular USB ports. It has an USB interface to communicate with USB host controller and is compliant with USB specification V1.1 and V2.0. It implements 10/100Mbps Ethernet LAN function based on IEEE802.3, and IEEE802.3u standards or HomePNA standard. It integrates an on-chip 10/100Mbps Ethernet PHY to simplify system design and provides an optional media-independent interface (MII) for implementing Fast Ethernet and HomePNA functions.

The AX88772 needs 12MHz clock for USB operation and 25Mhz clock for Fast Ethernet operation. It is in 128-pin LQFP low profile package with CMOS process and requires only single 3.3V power supply to operate.

1.2 AX88772 Block Diagram

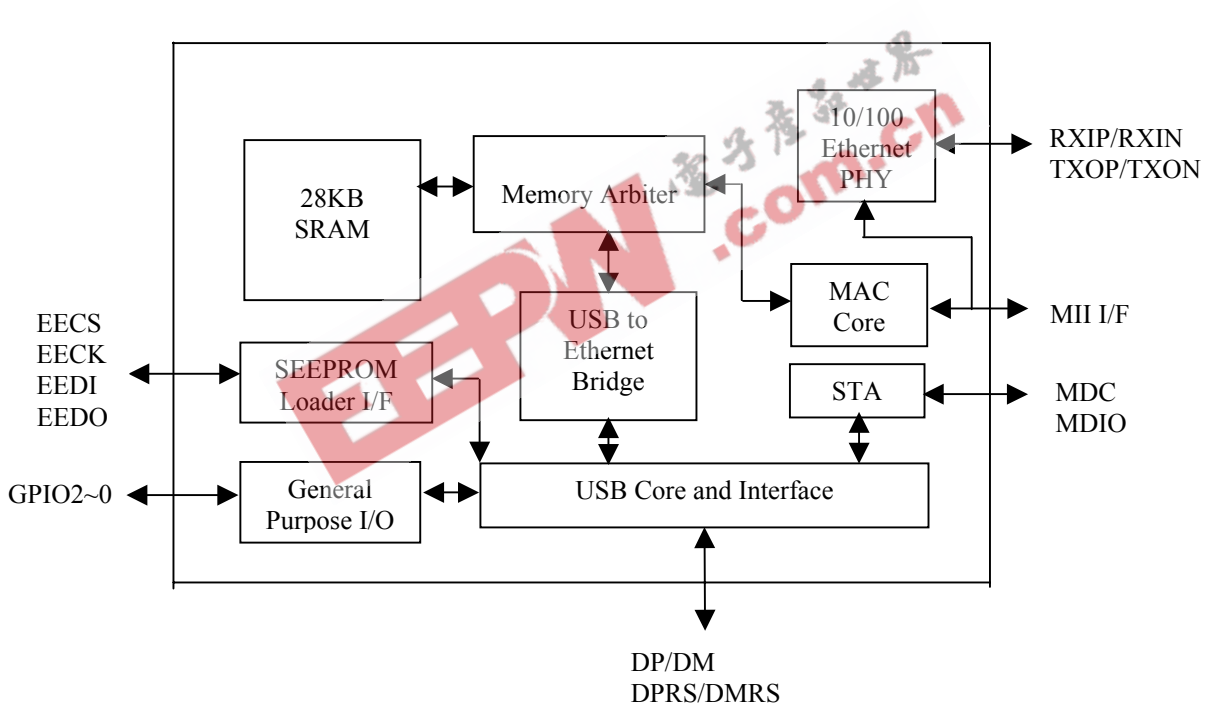


Figure 1: AX88772 Block Diagram

1.3 AX88772 Pinout Diagram

The AX88772 is housed in the 128-pin LQFP package.

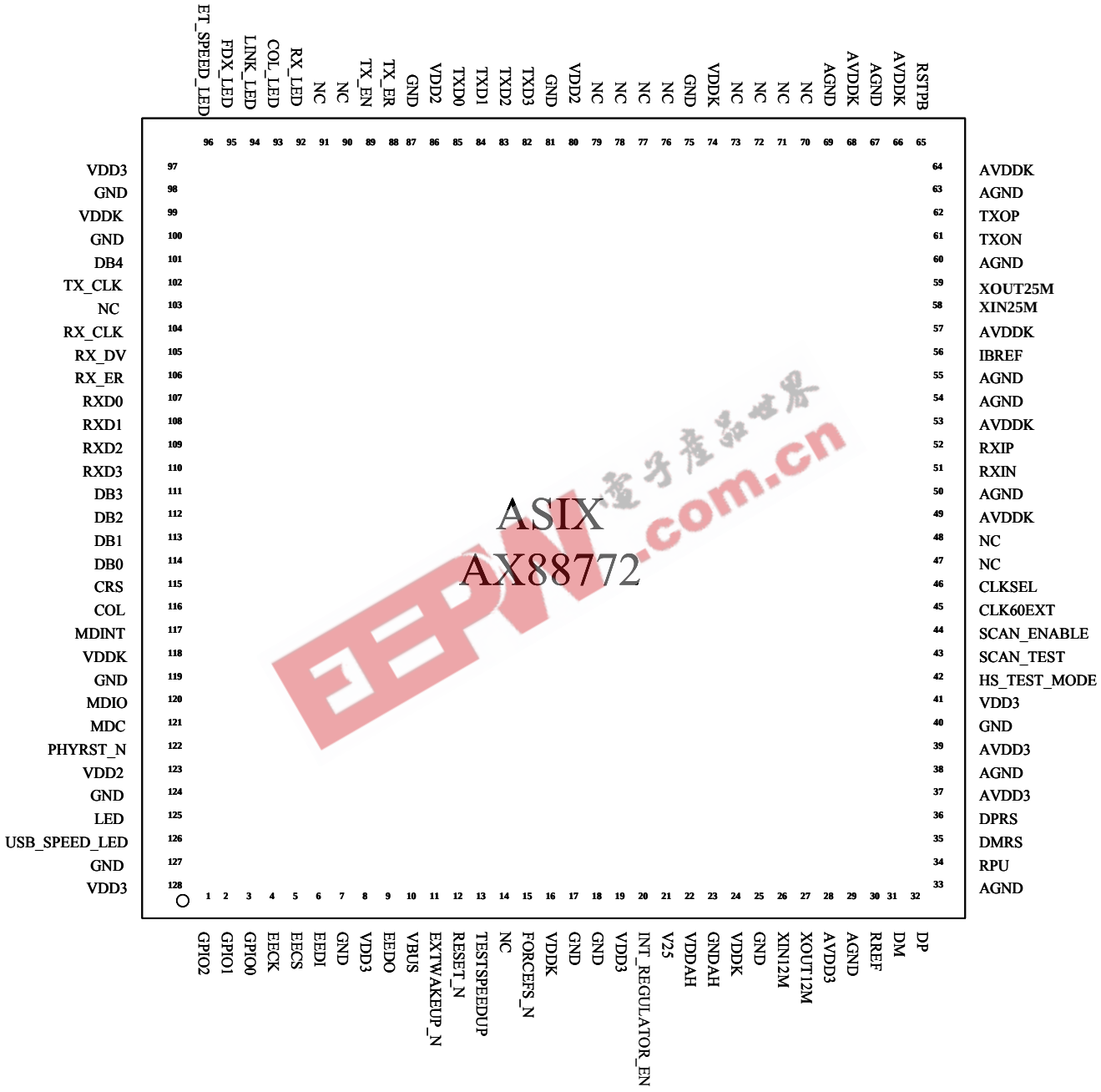


Figure 2: AX88772 Pinout Diagram

2.0 Signal Description

The following abbreviations apply to the following pin description table.

I2	**Input, 2.5V with 3.3V tolerant**	**B2**	**Bi-directional I/O, 2.5V with 3.3V tolerant**
I3	**Input, 3.3V**	**B5**	**Bi-directional I/O, 3.3V with 5V tolerant**
I5	**Input, 3.3V with 5V tolerant**	**PU**	**Internal Pull Up (75K)**
O2	**Output, 2.5V with 3.3V tolerant**	**PD**	**Internal Pull Down (75K)**
O3	**Output, 3.3V**	**P**	**Power Pin**
O5	**Output, 3.3V with 5V tolerant**	**S**	**Schmitt Trigger**
B	**Bi-directional I/O**		

Table 1: Pinout Description

Pin Name	Type	Pin No	Pin Description
USB Interface			
DP	B	32	USB 2.0 data positive pin.
DM	B	31	USB 2.0 data negative pin.
DPRS	B	36	USB 1.1 data positive pin. Please connect to DP through a 39ohm (+/-1%) serial resistor.
DMRS	B	35	USB 1.1 data negative pin. Please connect to DM through a 39ohm (+/-1%) serial resistor.
VBUS	I5/PD/S	10	VBUS pin input. Please connect to USB bus power.
XIN12M	I3	26	12Mhz crystal or oscillator clock input. This clock is needed for USB PHY transceiver to operate. The recommended operating frequency range is 12.000800Mhz ~12.004800Mhz.
XOUT12M	O3	27	12Mhz crystal or oscillator clock output.
RREF	I	30	For USB PHY's internal biasing. Please connect to AGND through a 12.1Kohm (+/-1%) resistor.
RPU	I	34	For USB PHY's internal biasing. Please connect to AVDD3 (3.3V) through a 1.5Kohm (+/-5%) resistor.
Station Management Interface			
MDC	O2	121	Station Management Data Clock output. The timing reference for MDIO. All data transfers on MDIO are synchronized to the rising edge of this clock. The frequency of MDC is 1.5MHz.
MDIO	B2/PU	120	Station Management Data Input/Output. Serial data input/output transfers from/to the PHYs. The transfer protocol conforms to the IEEE 802.3u MII spec.
MDINT	I2/PU	117	Station Management Interrupt input.
MII Interface			
RX_CLK	I2	104	Receive Clock. RX_CLK is received from PHY to provide timing reference for the transfer of RXD [7:0], RX_DV, and RX_ER signals on receive direction of MII interface.
RXD [3:0]	I2	110, 109, 108, 107	Receive Data. RXD [3:0] is driven synchronously with respect to RX_CLK by PHY.
RX_DV	I2	105	Receive Data Valid. RX_DV is driven synchronously with respect to RX_CLK by PHY. It is asserted high when valid data is present on RXD [3:0].
RX_ER	I2	106	Receive Error. RX_ER is driven synchronously with respect to RX_CLK by PHY. It is asserted high for one or more RX_CLK periods to indicate to the MAC that an error has detected.
COL	I2	116	Collision Detected. COL is driven high by PHY when the collision is detected.

CRS	I2	115	Carrier Sense. CRS is asserted high asynchronously by the PHY when either transmit or receive medium is non-idle.
TX_CLK	I2	102	Transmit Clock. TX_CLK is received from PHY to provide timing reference for the transfer of TXD [3:0], TX_EN and TX_ER signals on transmit direction of MII interface.
TXD [3:0]	O2	82, 83, 84, 85	Transmit Data. TXD [3:0] is transitioned synchronously with respect to the rising edge of TX_CLK.
TX_EN	O2	89	Transmit Enable. TX_EN is transitioned synchronously with respect to the rising edge of TX_CLK. TX_EN is asserted high to indicate a valid TXD [3:0].
TX_ER	O2	88	Transmit Coding Error. TX_ER is transitioned synchronously with respect to the rising edge of TX_CLK. When asserted high for one or more TX_CLK, the PHY shall emit one or more code-groups that are not part of the valid data or delimiter set somewhere in the frame being transmitted.
Serial EEPROM Interface			
EECK	O5	4	EEPROM Clock. EECK is an output clock to EEPROM to provide timing reference for the transfer of EECS, EEDI, and EEDO signals.
EECS	O5	5	EEPROM Chip Select. EECS is asserted high synchronously with respect to rising edge of EECK as chip select signal.
EEDI	O5	6	EEPROM Data In. EEDI is the serial output data to EEPROM's data input pin and is synchronous with respect to the rising edge of EECK.
EEDO	I5/PD	9	EEPROM Data Out. EEDO is the serial input data from EEPROM's data output pin.
Ethernet Phy Interface			
XIN25M	I	58	25Mhz crystal or oscillator clock input. This clock is needed for the embedded 10/100 Ethernet PHY to operate. The recommended reference frequency is 25Mhz +/-0.005%. This input pin is only 2.5V tolerant and should not apply 3.3V clock signal directly to this pin if an external oscillator is used.
XOUT25M	O	59	25Mhz crystal or oscillator clock output. This output pin is 2.5V tolerant.
RSTPB	I	65	Reset input of embedded Ethernet PHY: RSTPB is an active low input used for resetting internal Ethernet PHY. When internal Ethernet PHY is used, user can connect this pin to an external RC circuit, which gets pulled-up to AVDDK (2.5V). The reset period from 50ms to 150ms is recommended.
RXIP	I	52	Receive data input positive pin for both 10BASE-T and 100BASE-TX.
RXIN	I	51	Receive data input negative pin for both 10BASE-T and 100BASE-TX.
TXOP	O	62	Transmit data output positive pin for both 10BASE-T and 100 BASE-TX
TXON	O	61	Transmit data output negative pin for both 10BASE-T and 100 BASE-TX
IBREF	B	56	For Ethernet PHY's internal biasing. Please connect to GND through a 12.3Kohm resistor.
RX_LED	O3	92	Receive activity LED indicator. This pin drives low and high in turn (blinking) when Ethernet PHY is receiving and drives high when not receiving.
COL_LED	O3	93	Collision detected LED indicator. This pin drives low when the Ethernet PHY detects collision and drives high when no collision.
LINK_LED	O3	94	Link status LED indicator. This pin drives low continuously when the Ethernet link is up and drives low and high in turn (blinking) when Ethernet PHY is in receiving or transmitting state.
FDX_LED	O3	95	Full-Duplex LED indicator. This pin drives low when the Ethernet PHY is in full-duplex mode and drives high when in half duplex mode.

ET_SPEED_LED	O3	96	Ethernet speed LED indicator. This pin drives low when the Ethernet PHY is in 100BASE-TX mode and drives high when in 10BASE-T mode.
Misc. Pins			
RESET_N	I5/PU/S	12	Chip Reset Input. RESET_N pin is active low. When asserted, it puts the entire chip into reset state immediately. After completing reset, EEPROM data will be loaded automatically.
EXTWAKEUP_N	I5/PU/S	11	Remote-wakeup trigger from external pin. EXTWAKEUP_N should be asserted low for more than 2 cycles of 12MHz clock to be effective. For
GPIO [2:0]	B5/PD	1, 2, 3	General Purpose Input/ Output Pins. These pins are default as input pins after power-on reset. Please use GPIO0 for controlling the power down pin of external Ethernet Phy, if applicable.
PHYRST_N	O2	122	PHYRST_N is a tri-state output used for resetting external Ethernet PHY. This pin is default in tri-state after power-on reset. If external Ethernet PHY's reset level is active low, connect this to PHY's reset pin with a pulled-down resistor. If it's active high, connect this to PHY with a pulled-up resistor. This way can make sure the external Ethernet PHY stays in reset state before software brings it out of reset.
FORCEFS_N	I3/PU	15	Force USB Full Speed (active low). For normal operation, user should keep this pin NC to enable USB High Speed handshaking process to decide the speed of USB bus. Setting this pin low sets the device to operate at Full speed mode only and disables Chirp K (HS handshaking process).
LED	O3	125	LED indicator: When USB bus is in Full speed, this pin drives high continuously. When USB bus is in High speed, this pin drives low continuously. This pin drives high and low in turn (blinking) to indicate TX data transfer going on whenever the host controller sends bulk out data transfer.
USB_SPEED_LED	O3	126	USB bus speed LED indicator. When USB bus is in Full speed, this pin drives high continuously. When USB bus is in High speed, this pin drives low continuously.
TESTSPEEDUP	I3/PD	13	Test pin. For normal operation, user should keep this pin NC.
HS_TEST_MODE	I3/PD	42	Test pin. For normal operation, user should keep this pin NC.
SCAN_TEST	I3/PD	43	Test pin. For normal operation, user should keep this pin NC.
SCAN_ENABLE	I3/PD	44	Test pin. For normal operation, user should keep this pin NC.
CLK60EXT	I3/PD	45	Test pin. For normal operation, user should keep this pin NC.
CLKSEL	I3/PD	46	Test pin. For normal operation, user should keep this pin NC.
DB [4:0]	I2	101, 111, 112, 113, 114	Debug pins. For normal operation, user should set these pins low.
On-chip Regulator Pins			
INT_REGULATOR_EN	I	20	On-chip 3.3V to 2.5V voltage regulator enable. Connect this pin to VDDAH directly to enable on-chip regulator. Connect this pin to GNDAH to disable on-chip regulator.
VDDAH	P	22	3.3V Power supply to on-chip 3.3V to 2.5V voltage regulator.
GNDAH	P	23	Ground pin of on-chip 3.3V to 2.5V voltage regulator.
V25	P	21	2.5V voltage output of on-chip 3.3V to 2.5V voltage regulator.
Power and Ground Pins			
VDDK	P	16, 24, 74, 99, 118	Digital Core Power. 2.5V.
VDD2	P	80, 86, 123	Digital I/O Power. 2.5V.
VDD3	P	8, 19, 41, 97, 128	Digital I/O Power. 3.3V.

GND	P	7, 17, 18, 25, 40, 75, 81, 87, 98, 100, 119, 124, 127	Digital Ground.
AVDDK	P	49, 53, 57, 64, 66, 68	Analog Core Power. 2.5V.
AVDD3	P	28, 37, 39	Analog I/O Power. 3.3V.
AGND	P	29, 33, 38, 50, 54, 55, 60, 63, 67, 69	Analog Ground.

3.0 Function Description

3.1 USB Core and Interface

The USB core and interface contains an USB 2.0 transceiver, serial interface engine (SIE), USB bus protocol handshaking block, USB standard command, vendor command registers, logic for supporting bulk transfer, and interrupt transfer, etc. The USB interface is used to communicate with USB host controller and is compliant with USB specification V1.1 and V2.0.

3.2 10/100 Ethernet PHY

The 10/100 Fast Ethernet PHY is compliant with IEEE 802.3 and IEEE 802.3u standards. It contains an on-chip crystal oscillator, PLL-based clock multiplier, digital phase-locked loop for data/timing recovery. It provides over-sampling mixed-signal transmit drivers complying with 10/100BASE-TX transmit wave shaping / slew rate control requirements. It has robust mixed-signal loop adaptive equalizer for receiving signal recovery. It contains baseline wander corrective block to compensate data dependent offset due to AC coupling transformers. It supports auto-negotiation and has multi-function LED outputs.

3.3 MAC Core

The MAC core supports 802.3 and 802.3u MAC sub-layer functions, such as basic MAC frame receive and transmit, CRC checking and generation, filtering, forwarding, flow-control in full-duplex mode, and collision-detection and handling in half-duplex mode, etc. It provides a media-independent interface (MII) for implementing Fast Ethernet and HomePNA functions.

The MAC core interfaces to both external MII interface I/O pins and MII interface of the embedded 10/100 Ethernet PHY. The selection between the two MII interfaces is done via USB vendor command, Software PHY Select register. Figure 3 shows the datapath diagram of 10/100 Ethernet PHY and MII interface to MAC core.

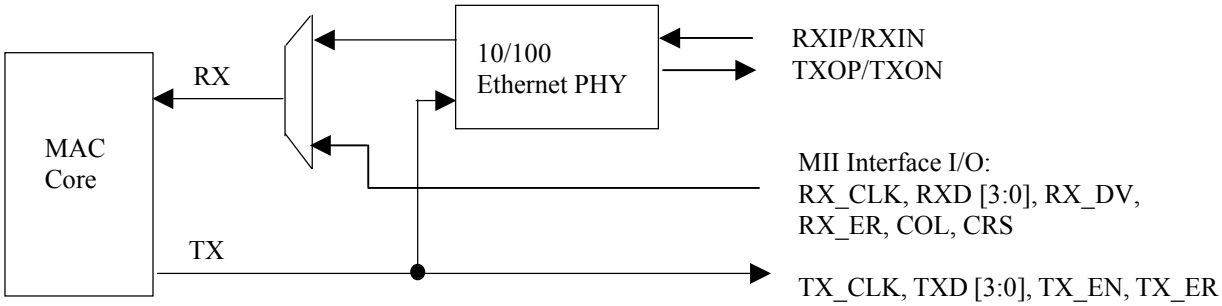


Figure 3: Internal Datapath Diagram of 10/100 Ethernet PHY and MII Interface

3.4 Station Management (STA)

The station management interface provides a simple, two-wire, serial interface to connect to a managed PHY device for the purposes of controlling the PHY and gathering status from the PHY. The station management interface allows

communicating with multiple PHY devices at the same time by identifying the managed PHY with 5-bit, unique Phy ID. The Phy ID of the embedded 10/100 Ethernet PHY is being pre-assigned to "1_0000".

Figure 4 shows the internal control mux for the station management interface. When doing read, the "mdin" signal will be driven from 10/100 Ethernet PHY only if Phy ID matches with "1_0000", otherwise, it will always be driven from external MDIO pin of the ASIC.

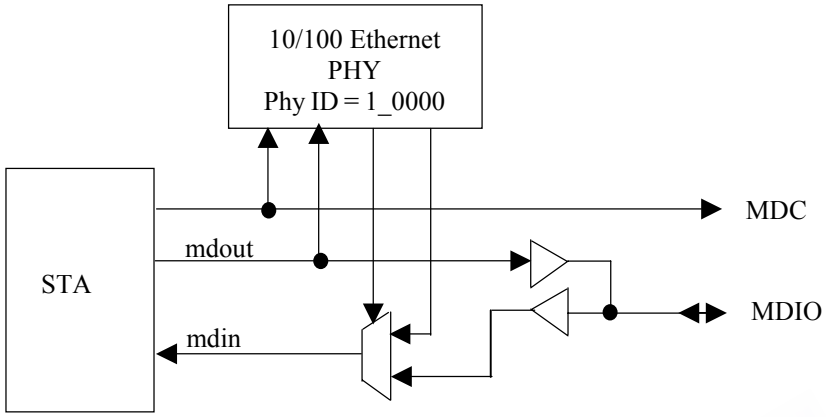


Figure 4: Internal Control Mux for Station Management Interface

3.5 Memory Arbiter

The memory arbiter block is responsible for storing received MAC frames into on-chip SRAM (packet buffer) and then forwarding to USB bus upon request from USB host via bulk in transfer. It also monitors packet buffer usage in full-duplex mode for triggering PAUSE frame transmission out on TX direction. The memory arbiter block is also responsible for storing MAC frames received from USB host via bulk out transfer and waiting to be transmitted out towards Ethernet network.

3.6 USB to Ethernet Bridge

The USB to Ethernet bridge block is responsible for converting Ethernet MAC frame into USB packets or vice-versa. This block supports proprietary burst transfer mechanism (submitted for US patent application) to offload software burden and to offer very high packet transfer throughput over USB bus.

3.7 Serial EEPROM Loader

The serial EEPROM loader is responsible for reading configuration data automatically from external serial EEPROM after power-on reset.

3.8 General Purpose I/O

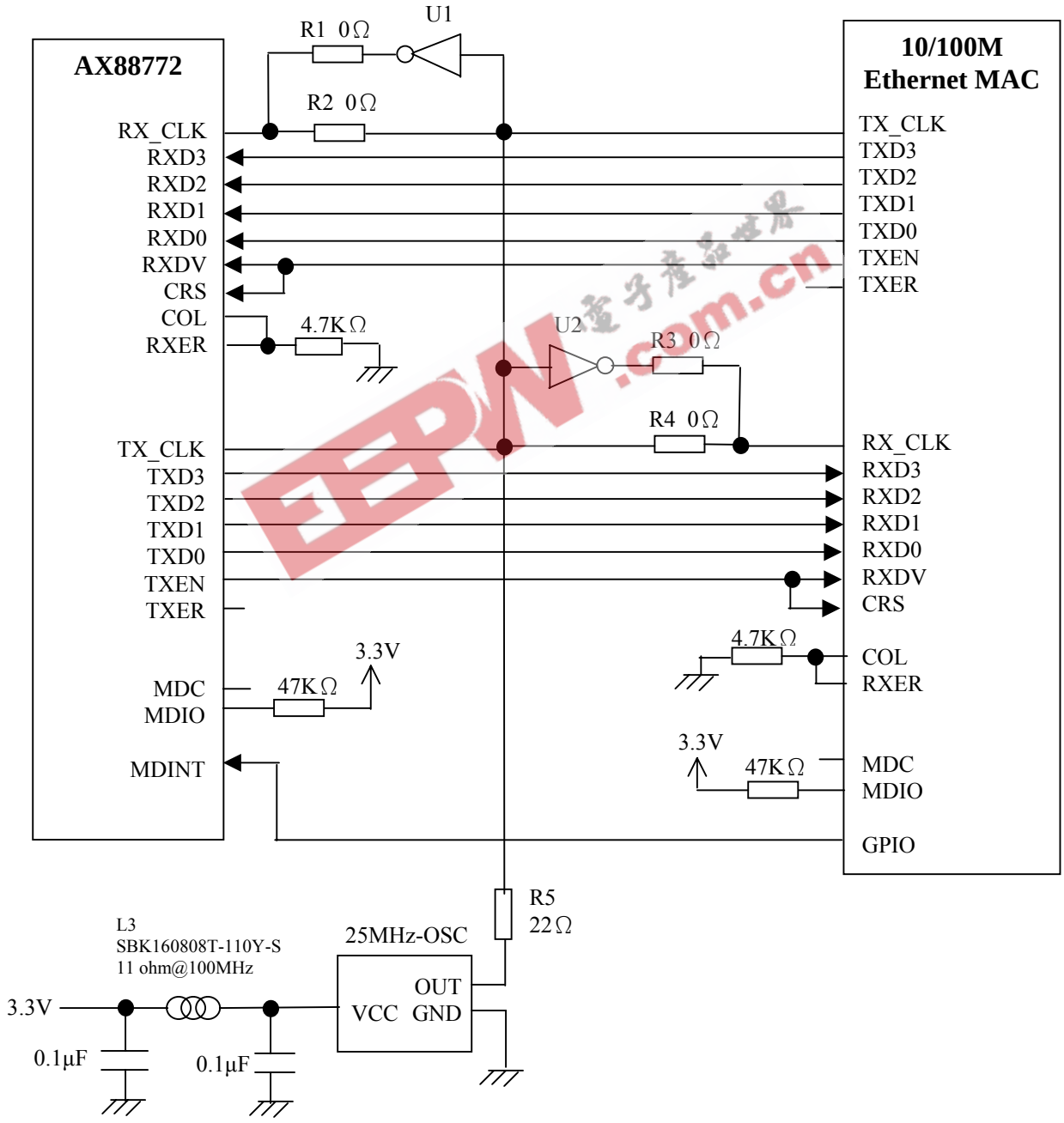
There are 3 general purpose I/O pins provided by this ASIC.

3.9 MAC to MAC Connection via MII Interface

Below figure shows recommended MAC-to-MAC connection for AX88772 MII Interfacing with an external Ethernet MAC device. When operating at this mode, the Ethernet MAC on both sides should be set to operate at 100M full-duplex mode.

The U1 & R1 are reserved for adjusting RXDV/RXD[3:0] input setup/hold time with respect to AX88772 RX_CLK clock phase. Either R2 or R1 is installed at a time. User should check the TX_CLK, TXD[3:0], TXEN output timing of external Ethernet MAC device vs. AX88772's RXDV/RXD[3:0] input setup/hold time.

The U2 & R3 are reserved for adjusting RXDV/RXD[3:0] input setup/hold time with respect to RX_CLK clock phase on external Ethernet MAC device. Either R3 or R4 is installed at a time. User should check the TX_CLK, TXD[3:0], TXEN output timing of AX88772 vs. the RXDV/RXD[3:0] setup/hold time of external Ethernet MAC device.



4.0 Serial EEPROM Memory Map

EEPROM OFFSET	HIGH BYTE	LOW BYTE
00H	Reserved	Word Count For Preload
01H	Flag	
02H	Length of High-Speed Device Descriptor (bytes)	EEPROM Offset of High-Speed Device Descriptor
03H	Length of High-Speed Configuration Descriptor (bytes)	EEPROM Offset of High-Speed Configuration Descriptor
04H	Node ID 1	Node ID 0
05H	Node ID 3	Node ID 2
06H	Node ID 5	Node ID 4
07H	Language ID High Byte	Language ID Low Byte
08H	Length of Manufacture String (bytes)	EEPROM Offset of Manufacture String
09H	Length of Product String (bytes)	EEPROM Offset of Product String
0AH	Length of Serial Number String (bytes)	EEPROM Offset of Serial Number String
0BH	Length of Configuration String (bytes)	EEPROM Offset of Configuration String
0CH	Length of Interface 0 String (bytes)	EEPROM Offset of Interface 0 String
0DH	Length of Interface 1/0 String (bytes)	EEPROM Offset of Interface 1/0 String
0EH	Length of Interface 1/1 String (bytes)	EEPROM Offset of Interface 1/1 String
0FH	Phy Register Offset for Interrupt Endpoint	Phy Register Offset for Interrupt Endpoint
10H	Max Packet Size High Byte	Max Packet Size Low Byte
11H	Secondary Phy_Type [7:5] and Phy_ID [4:0]	Primary Phy_Type [7:5] and Phy_ID [4:0]
12H	Pause Frame High Water Mark	Pause Frame Low Water Mark
13H	Length of Full-Speed Device Descriptor (bytes)	EEPROM Offset of Full-Speed Device Descriptor
14H	Length of Full-Speed Configuration Descriptor (bytes)	EEPROM Offset of Full-Speed Configuration Descriptor
15H-1FH	Reserved	Reserved

Table 2: Serial EEPROM Memory Map

4.1 Detailed Description

The following sections provide detailed description for some of the field in serial EEPROM memory map, for other fields not covered here, please refer to AX88772 EEPROM user guide for more details.

4.1.1 Word Count for Preload (00h)

The number of words to be preloaded by the EEPROM loader = 15h.

4.1.2 Flag (01h)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reserved						TDPE	CEM
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TACE	RDCE	SCPR	DCK	1	RWU	Reserved	SP

SP: Self-Power (for USB GetStatus)
1: Self power.
0: Bus power.
RWU: Remote Wakeup support.
1: Indicate that this device supports Remote Wakeup.
0: Not support.
DCK: Disable Chirp K.
1: Disabled.
0: Enable.
SCPR: Software Control PHY Reset.
1: The PRL and PRTE bits of Software Reset Register control the PHYRST_N output level.
0: The USB reset on USB bus and PRTE bit of Software Reset Register control the PHYRST_N output level.
RDCE: RX Drop CRC Enable.
1: CRC byte is dropped on received MAC frame forwarding to host.
0: CRC byte is not dropped.
TACE: TX Append CRC Enable.
1: CRC byte is generated and appended by the ASIC for every transmitted MAC frame.
0: CRC byte is not appended.
CEM: Capture Effective Mode.
1: Capture effective mode enable.
0: Disabled.
TDPE: Test Debug Port Enable.
1: Enable test debug port for chip debug purpose.
0: Disable test debug port and the chip operate in normal function mode
Bit 1, 10~15: Reserved.

4.1.3 Node ID (04~06h)

The Node ID 0 to 5 bytes represent the MAC address of the device, for example, if MAC address = 01-23-45-67-89-ABh, then Node ID 0 = 01, Node ID 1 = 23, Node ID 2 = 45, Node ID 3 = 67, Node ID 4 = 89, and Node ID 5 = AB.

4.1.4 Phy Register Offset for Interrupt Endpoint (0Fh)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reserved			Phy Register Offset 1				
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved			Phy Register Offset 2				

Phy Register Offset 1: Fill in Phy's Register Offset of Primary Phy here. Upon each Interrupt Endpoint issued, its register value will be reported in byte# 5 and 6 of Interrupt Endpoint packet.
Phy Register Offset 2: Fill in Phy's Register Offset of Primary Phy here. Upon each Interrupt Endpoint issued, its register value will be reported in byte# 7 and 8 of Interrupt Endpoint packet.

4.1.5 Max Packet Size High/Low Byte (10h)

Fill in this field the maximum RX/TX MAC frame size supported by this ASIC. The number must be even number in terms of byte and should be less than or equal to 2500 bytes.

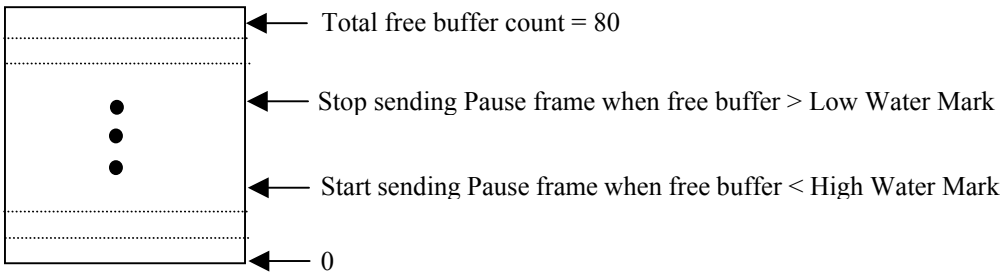
4.1.6 Primary/Secondary Phy_Type and Phy_ID (11h)

The 3 bits Phy_Type field for both Primary and Secondary Phy is defined as follows,
3'b000: 10/100 Ethernet Phy or 1M HOME Phy.
3'b111: non-supported Phy. For example, the High Byte value of "E0h" means that secondary Phy is not supported.

Note that the Phy_ID of the embedded 10/100 Ethernet PHY is being assigned to 5'b1_0000.

4.1.7 Pause Frame High Water and Low Water Mark (12H)

When operating in full-duplex mode, correct setting of this field is very important and can affect the overall packet receive throughput performance in a great deal. The High Water Mark is the threshold to trigger sending of Pause frame and the Low Water Mark is the threshold to stop sending of Pause frame. Note that each free buffer count here represents 256 bytes of packet storage space in SRAM.



4.1.8 Power-Up Steps

After power-on reset, the ASIC will automatically perform following steps to the Ethernet Phys via MDC/MDIO lines,

1. Write to Phy_ID of 00h with Phy register offset 00h to power down all Phys attached to station management interface.
2. Write to Primary Phy_ID with Phy register offset 00h to power down Primary Phy.
3. Write to Secondary Phy_ID with Phy register offset 00h to power down Secondary Phy.

5.0 USB Configuration Structure

5.1 USB Configuration

The AX88772 supports 1 Configuration only.

5.2 USB Interface

The AX88772 supports 1 interface.

5.3 USB Endpoints

The AX88772 supports following 4 endpoints:

Endpoint 0: Control endpoint. It is used for configuring the device, e.g., standard commands and vendor commands, etc.

Endpoint 1: Interrupt endpoint. It is used for reporting status.

Endpoint 2: Bulk In endpoint. It is used for receiving Ethernet Packet.

Endpoint 3: Bulk Out endpoint. It is used for transmitting Ethernet Packet.

6.0 USB Commands

There are three command groups for Endpoint 0 (Control Endpoint) in AX88772:

- The USB standard commands
- The USB vendor commands
- The USB Communication Class commands

6.1 USB Standard Commands

- The Language ID is 0x0904 for English
- PPLL means buffer length
- CC means configuration number
- I I means Interface number
- AA means Device Address

Setup Command	Data Bytes	Access Type	Description
8006_00 01 00 00 LLPP	PPLL bytes in Data stage	Read	Get Device Descriptor
8006_0002 0000_LLPP	PPLL bytes in Data stage	Read	Get Configuration Descriptor
8006_0003_0000_LLPP	PPLL bytes in Data stage	Read	Get Supported Language ID
8006_0103_0904_LLPP	PPLL bytes in Data stage	Read	Get Manufacture String
8006_0203_0904_LLPP	PPLL bytes in Data stage	Read	Get Product String
8006_0303_0904_LLPP	PPLL bytes in Data stage	Read	Get Serial Number String
8006_0403_0904_LLPP	PPLL bytes in Data stage	Read	Get Configuration String
8006_0503_0904_LLPP	PPLL bytes in Data stage	Read	Get Interface 0 String
8006_0603_0904_LLPP	PPLL bytes in Data stage	Read	Get Interface 1/0 String
8006_0703_0904_LLPP	PPLL bytes in Data stage	Read	Get Interface 1/1 String
8008_0000_0000_0100	1 bytes in Data stage	Read	Get Configuration
0009_CC00_0000_0000	No data in Data stage	Write	Set Configuration
810A_0000 _I I00_0100	1 bytes in Data stage	Read	Get Interface
010B_AS00_0000_0000	No data in Data stage	Write	Set Interface
0005_AA00_0000_0000	No data in Data stage	Write	Set Address

Table 3: USB Standard Command Register Map

6.2 USB Vendor Commands

No	Setup Command	Data Bytes	Access Type	Description
1.	C002_AA0B_0C00_0800	8 bytes in Data stage	Read	Rx/Tx SRAM Read Register
2.	4003_AA0B_0C00_0800	8 bytes in Data stage	Write	Rx/Tx SRAM Write Register
3.	4006_0000_0000_0000	No data in Data stage	Write	Software Serial Management Control Register
4.	C007_ AA00_CC00_0200	2 bytes in Data stage	Read	PHY Read Register
5.	4008 _AA00_CC00_0200	2 bytes in Data stage	Write	PHY Write Register
6.	C009_0000_0000_0100	1 bytes in Data stage	Read	Serial Management Status Register
7.	400A_0000_0000_0000	No data in Data stage	Write	Hardware Serial Management Control Register
8.	C00B_AA00_0000_0200	2 bytes in Data stage	Read	SROM Read Register
9.	400C_AA00_CCDD_0000	No data in Data stage	Write	SROM Write Register
10.	400D_0000_0000_0000	No data in Data stage	Write	SROM Write Enable Register
11.	400E_0000_0000_0000	No data in Data stage	Write	SROM Write Disable Register
12.	C00F_0000_0000_0200	2 bytes in Data stage	Read	Rx Control Register
13.	4010_AABB_0000_0000	No data in Data stage	Write	Rx Control Register
14.	C011_0000_0000_0300	3 bytes in Data stage	Read	IPG/IPG1/IPG2 Register
15.	4012_AABB_CC00_0000	No data in Data stage	Write	IPG/IPG1/IPG2 Register
16.	C013_0000_0000_0600	6 bytes in Data stage	Read	Node ID Register
17.	4014_0000_0000_0600	6 bytes in Data stage	Write	Node ID Register
18.	C015_0000_0000_0800	8 bytes, *MA0~MA7*, in Data stage	Read	Multicast Filter Array Register
19.	4016_0000_0000_0800	8 bytes, *MA0~MA7*, in Data stage	Write	Multicast Filter Array Register
20.	4017_AA00_0000_0000	No data in Data stage	Write	Test Register
21.	C019_0000_0000_0200	2 bytes in Data stage	Read	Ethernet/HomePNA Phy Address Register
22.	C01A_0000_0000_0200	2 bytes in Data stage	Read	Medium Status Register
23.	401B_AABB_0000 _0000	No data in Data stage	Write	Medium Mode Register
24.	C01C_0000_0000_0100	1bytes in Data stage	Read	Monitor Mode Status Register
25.	401D_AA00_0000_0000	No data in Data stage	Write	Monitor Mode Register
26.	C01E _0000_0000_0100	1 bytes in Data stage	Read	GPIOs Status Register
27.	401F_AA00_0000_0000	No data in Data stage	Write	GPIOs Register
28.	4020_AA00_0000_0000	No data in Data stage	Write	Software Reset Register
29.	C021_AA00_0000_0100	1 bytes in Data stage	Read	Software PHY Select Status Register
30.	4022_AA00_0000_0000	No data in Data stage	Write	Software PHY Select Register

Table 4: USB Vendor Command Register Map

6.2.1 Detailed Register Description

6.2.1.1 Rx/Tx SRAM Read Register (02h, read only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AA [7:0]							
Reserved				B [3:0]			
0h				C [3:0]			
DD [7:0] in Data stage							
EE [7:0] in Data stage							
FF [7:0] in Data stage							
GG [7:0] in Data stage							
HH [7:0] in Data stage							
II [7:0] in Data stage							
JJ [7:0] in Data stage							
KK [7:0] in Data stage							

{B [3:0], AA [7:0]}: The read address of RX or TX SRAM.
C [0]: RAM selection.
0: indicates to read from RX SRAM.
1: indicates to read from TX SRAM.
C [3:1]: Reserved.
{DD [7:0], EE [7:0], FF [7:0], GG [7:0], HH [7:0], II [7:0], JJ [7:0], KK [7:0]}: The 64-bits of data presented in Data stage are the data to be written to RX or TX SRAM.

6.2.1.2 Rx/Tx SRAM Write Register (03h, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AA [7:0]							
Reserved				B [3:0]			
Reserved				C [3:0]			
DD [7:0] in Data stage							
EE [7:0] in Data stage							
FF [7:0] in Data stage							
GG [7:0] in Data stage							
HH [7:0] in Data stage							
II [7:0] in Data stage							
JJ [7:0] in Data stage							
KK [7:0] in Data stage							

{B [3:0], AA [7:0]}: The write address of RX or TX SRAM.
C [0]: RAM selection.
0: indicates to write to RX SRAM.
1: indicates to write to TX SRAM.
C [3:1]: Reserved.
{DD [7:0], EE [7:0], FF [7:0], GG [7:0], HH [7:0], II [7:0], JJ [7:0], KK [7:0]}: The 64-bits of data presented in Data stage are the data to be written to RX or TX SRAM.

6.2.1.3 Software Serial Management Control Register (06h, write only)

When software needs to access to Ethernet PHY's internal registers, one has to first issue this command to request the ownership of Serial Management Interface. The ownership status of the interface can be retrieved from Serial Management Status Register.

6.2.1.4 PHY Read Register (07h, read only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AA [7:0]							
00h							
CC [7:0]							

AA [4:0]: The PHY ID value.
CC [4:0]: The register address of Ethernet PHY's internal register.
AA [7:5]: Reserved
CC [7:5]: Reserved

6.2.1.5 PHY Write Register (08h, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AA [7:0]							
00h							
CC [7:0]							

AA [4:0]: The PHY ID value.
CC [4:0]: The register address of Ethernet PHY's internal register.
AA [7:5]: Reserved
CC [7:5]: Reserved

6.2.1.6 Serial Management Status Register (09h, read only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved							Host_EN

Host_EN: Host access Enable. Software can read this register to determine the current ownership of Serial Management Interface.
1: Software is allowed to access Ethernet PHY's internal registers via PHY Read Register or PHY Write Registers.
0: ASIC's hardware owns the Serial Management Interface and software's access is ignored.

6.2.1.7 Hardware Serial Management Control Register (0Ah, write only)

When software is done accessing Serial Management Interface, one needs to issue this command to release the ownership of the Interface back to ASIC's hardware. After issuing this command, following PHY Read Register or PHY Write Register from software will be ignored. **NOTE**: Software should issue this command every time after finished accessing Serial Management Interface to release the ownership back to hardware to allow periodic Interrupt Endpoint to be able to access the Ethernet PHY's registers via the Serial Management Interface.

6.2.1.8 SROM Read Register (0Bh, read only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AA [7:0]							

AA [7:0]: The read address of Serial EEROM.

6.2.1.9 SROM Write Register (0Ch, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AA [7:0]							
00h							
CC [7:0]							
DD [7:0]							

AA [7:0]: The write address of Serial EEROM.
{ DD [7:0], CC [7:0] }: The write data value of Serial EEROM

6.2.1.10 Write SROM Enable (0Dh, write only)

User issues this command to enable write permission to Serial EEPROM from SROM Write Register.

6.2.1.11 Write SROM Disable (0Eh, write only)

User issues this command to disable write permission to Serial EEPROM from SROM Write Register.

6.2.1.12 Rx Control Register (0Fh, read only and 10h, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SO	Reserved	AP	AM	AB	SEP	AMALL	PRO
0h				Reserved		MFB [1:0]	

AA [7:0] = { SO, Reserved, AP, AM, AB, Reserved, AMALL, PRO }
BB [7:0] = { 0h, Reserved [3:2], SB [1:0] }

PRO: PACKET_TYPE_PROMISCUOUS.
1: All frames received by the ASIC are forwarded up toward the host.
0: Disabled (default).
AMALL: PACKET_TYPE_ALL_MULTICAST.
1: All multicast frames received by the ASIC are forwarded up toward the host, not just the frames whose scrambling result of DA matching with multicast address list provided in Multicast Filter Array Register.
0: Disabled. This only allows multicast frames whose scrambling result of DA field matching with multicast address list provided in Multicast Filter Array Register to be forwarded up toward the host (default).
SEP: Save Error Packet.
1: Received packets with CRC error are saved and forwarded to the host anyway.
0: Received packets with CRC error are discarded automatically without forwarding to the host (default).
AB: PACKET_TYPE_BROADCAST.
1: All broadcast frames received by the ASIC are forwarded up toward the host (default).
0: Disabled.
AM: PACKET_TYPE_MULTICAST.
1: All multicast frames whose scrambling result of DA matching with multicast address list are forwarded up to the host (default).
0: Disabled.
AP: Accept Physical Address from Multicast Filter Array.
1: Allow unicast packets to be forwarded up toward host if the lookup of scrambling result of DA is found within multicast address list.
0: Disabled, that is, unicast packets filtering are done without regarding multicast address list (default).
SO: Start Operation.
1: Ethernet MAC start operating.
0: Ethernet MAC stop operating (default).

MFB [1:0]: Maximum Frame Burst transfer on USB bus.
00: 2048 Bytes
01: 4096 Bytes
10: 8192 Bytes
11: 16384 Bytes (default).

6.2.1.13 IPG/IPG1/IPG2 Control Register (11h, read only and 12h, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AA [7:0]							
BB [7:0]							
CC [7:0]							

AA [6:0] = IPG [6:0].
BB [6:0] = IPG1 [6:0].
CC [6:0] = IPG2 [6:0].
IPG [6:0]: Inter Packet Gap for back-to-back transfer on TX direction in MII mode (default = 15h).
IPG1 [6:0]: IPG part1 value (default = 0Ch).
IPG2 [6:0]: IPG part1 value + part2 value (default = 12h).
AA [7]: Reserved.
BB [7]: Reserved.
CC [7]: Reserved.

6.2.1.14 Node ID Register (13h, read only and 14h, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AA [7:0]							
BB [7:0]							
CC [7:0]							
DD [7:0]							
EE [7:0]							
FF [7:0]							

AA [7:0] = NOID 0.
BB [7:0] = NOID 1.
CC [7:0] = NOID 2.
DD [7:0] = NOID 3.
EE [7:0] = NOID 4.
FF [7:0] = NOID 5.
{FF [7:0], EE [7:0], DD [7:0], CC [7:0], BB [7:0], AA [7:0]} = Ethernet MAC address [47:0] of the node.

6.2.1.15 Multicast Filter Array (15h, read only and 16h, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MA 0 [7:0]							
MA 1 [7:0]							
MA 2 [7:0]							
MA 3 [7:0]							
MA 4 [7:0]							
MA 5 [7:0]							
MA 6 [7:0]							
MA 7 [7:0]							

{MA7 [7:0], MA6 [7:0], MA5 [7:0], MA4 [7:0], MA3 [7:0], MA2 [7:0], MA1 [7:0], MA0 [7:0]} = the multicast address bit map for multicast frame filtering block. See Figure 5: Multicast Filter Example, for example.

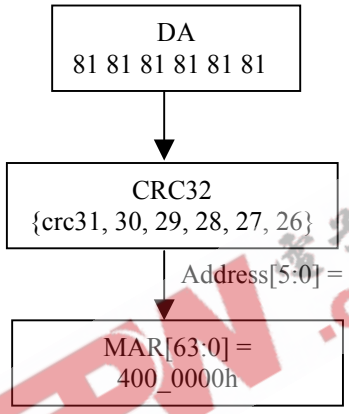


Figure 5: Multicast Filter Example

6.2.1.16 Test Register (17h, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MM [7:6]							LDRND

LDRND: Load Random number into MAC's exponential back-off timer. User writes a "1" to enable the ASIC to load a small random number into MAC's back-off timer to shorten the back-off duration in each retry after collision. This register is used for test purpose. Default value = 0.

MM [7:6]: Reserved.

6.2.1.17 Ethernet / HomePNA Phy Address Register (19h, read only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SecPhyType [2:0]			SecPhyID [4:0]				
PriPhyType [2:0]			PriPhyID [4:0]				

SecPhyType, SecPhyID: The Secondary PHY address loaded from serial EEPROM's offset address 11h.
PriPhyType, PriPhyID: The Primarily PHY address loaded from serial EEPROM's offset address 11h.

6.2.1.18 Medium Status Register (1Ah, read only) and Medium Mode Register (1Bh, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PF	0	TFC	RFC	0	1	FD	0
Reserved			SM	SBP	Reserved	PS	RE

AA [7:0] = {PF, JFE, TFC, RFC, EN125, AC, FD, GM}.
BB [7:0] = {Reserved, SM, SBP, JE, PS, RE}.
Bit 0: Please always write 0 to this bit.
PS: Port Speed in MII mode
1: 100 Mbps (default).
0: 10 Mbps.
FD: Full Duplex mode
1: Full Duplex mode (default).
0: Half Duplex mode.
Bit 2: Please always write 1 to this bit.
Bit 3: Please always write 0 to this bit.
RFC: RX Flow Control enable.
1: Enable receiving of pause frame on RX direction during full duplex mode (default).
0: Disabled.
TFC: TX Flow Control enable.
1: Enable transmitting pause frame on TX direction during full duplex mode (default).
0: Disabled.
Bit 6: Please always write 0 to this bit.
PF: Check only "length/type" field for Pause Frame.
1: Enable, i.e., Pause frames are identified only based on L/T filed.
0: Disabled, i.e., Pause frames are identified based on both DA and L/T fields (default).
RE: Receive Enable.
1: Enable RX path of the ASIC.
0: Disabled (default).
SBP: Stop Backpressure.
1: When TFC bit = 1, setting this bit enables backpressure on TX direction "continuously" during RX buffer full condition in half duplex mode.
0: When TFC bit = 1, setting this bit enable backpressure on TX direction "intermittently" during RX buffer full condition in half duplex mode (default).
SM: Super Mac support.
1: Enable Super Mac to shorten exponential back-off time during transmit retry.
0: Disabled (default).

6.2.1.19 Monitor Mode Status Register (1Ch, read only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved			US	Reserved	RWMP	RWLU	MOM

MOM: Monitor Mode.
1: Enable. All received packets will be checked on DA and CRC but not buffered into memory.
0: Disabled (default).
RWLU: Remote Wakeup trigger by Ethernet Link-up.
1: Enable
0: Disabled (default).
RWMP: Remote Wakeup trigger by Magic Packet.
1: Enable
0: Disabled (default).
US: USB Speed.
1: High speed mode.
0: FS speed mode.

6.2.1.20 Monitor Mode Register (1Dh, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved					RWMP	RWLU	MOM

MOM: Monitor Mode.
1: Enable. All received packets will be checked on DA and CRC but not buffered into memory.
0: Disabled (default).
RWLU: Remote Wakeup trigger by Ethernet Link-up.
1: Enable.
0: Disabled (default).
RWMP: Remote Wakeup trigger by Magic Packet.
1: Enable.
0: Disabled (default).
AA [7:3]: Reserved.

6.2.1.21 GPIO Status Register (1Eh, read only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		GPI_2	GPO_2_EN	GPI_1	GPO_1_EN	GPI_0	GPO_0_EN

GPO_0_EN: Current level of pin GPIO0's output enable.
GPI_0: Input level on GPIO0 pin when GPIO0 is as an input pin.
GPO_1_EN: Current level of pin GPIO1's output enable.
GPI_1: Input level on GPIO1 pin when GPIO1 is as an input pin.
GPO_2_EN: Current level of pin GPIO2's output enable.
GPI_2: Input level on GPIO2 pin when GPIO2 is as an input pin.

6.2.1.22 GPIO Register (1Fh, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSE		GPO_2	GPO2EN	GPO_1	GPO1EN	GPO_0	GPO0EN

GPO0EN: Pin GPIO0 Output Enable.
1: Output is enabled (meaning GPIO0 is used as an output pin).
0: Output is tri-stated (meaning GPIO0 is used as an input pin) (default).
GPO_0: Pin GPIO0 Output Value.
GPO1EN: Pin GPIO1 Output Enable.
1: Output is enabled (meaning GPIO1 is used as an output pin).
0: Output is tri-stated (meaning GPIO1 is used as an input pin) (default).
GPO_1: Pin GPIO1 Output Value.
0: (default).
GPO2EN: Pin GPIO2 Output Enable.
1: Output is enabled (meaning GPIO2 is used as an output pin).
0: Output is tri-stated (meaning GPIO2 is used as an input pin) (default).
GPO_2: Pin GPIO2 Output Value.
0: (default).
RSE: Reload Serial EEPROM.
1: Enable.
0: Disabled (default)

6.2.1.23 Software Reset Register (20h, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	IPPD	IPRL	BZ	PRL	PRTE	RT	RR

RR: Clear frame length error for Bulk In.
1: set high to clear state.
0: set low to exit clear state (default).
RT: Clear frame length error for Bulk Out.
1: set high to enter clear state.
0: set low to exit clear state (default).
PRTE: External Phy Reset pin Tri-state Enable.
1: Enable, i.e., the external PHYRST_N pin is tri-stated (default). This allows the PHYRST_N pin's active level to be controlled by external pulled-up (active high during power-on) or pulled-down resistor (active low during power-on).
0: Disabled, i.e., the external PHYRST_N pin's level is driven by either PRL bit or internal "USB RESET" based on the setting in SCPR bit in Flag byte of EEPROM.
PRL: External Phy Reset pin Level. When SCPR bit = 1 and PRTE = 0, this bit controls the output level of external PHYRST_N pin.
1: Set to high (default).
0: Set to low.
BZ: Force Bulk In to return a Zero-length packet.
1: Software can force Bulk In to return a zero-length USB packet.
0: Normal operation mode (default).
IPRL: Internal Phy Reset control. When SCPR bit = 1, this bit acts as reset signal of internal Ethernet Phy.
1: Internal Ethernet Phy is in operating state.
0: Internal Ethernet Phy in reset state (default).
IPPD: Internal Ethernet Phy Power Down control.
1: Internal Ethernet Phy is in power down mode (default).
0: Internal Ethernet Phy is in operating mode.

6.2.1.24 Software PHY Select Status Register (21h, read only) and Software PHY Select Register 22h, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved						ASEL	PSEL

PSEL: Phy Select, when ASEL = 0 (manually select the Phy to operate)
1: Select embedded 10/100 Ethernet Phy (default).
0: Select external Phy, which is attached to the MII interface
ASEL: Auto Select or Manual Select
1: Automatically select based on link status of embedded 10/100 Ethernet Phy (default).
0: Manually select between the embedded 10/100 Ethernet Phy and the external one.

6.2.2 Remote Wakeup Description

After AX88772 enters into suspend mode, either the USB host or AX88772 itself can awake it up and resume back to the original operation mode before it entered suspend. Following truth table shows the chip setting, wakeup event, and device response supported by this ASIC. Note that "X" stands for don't-care.

Wakeup by	Setting				Wakeup Event					Device awakes up?
	RWU bit of Flag byte in EEPROM	Set_Feature standard command	RWLU of Monitor Mode Register	RWMP of Monitor Mode register	Host send resume signal	Receiving Magic Packet	EXTWAKEUP_N pin	Linkup detected on Primary Phy	Linkup detected on Secondary Phy	
Host	X	X	X	X	J -> K					Yes
Device	0	0	X	X		X	X	X	X	No
Device	1	1	0	1		Yes				Yes
Device	1	1	1	0				Yes		Yes
Device	1	1	1	0					Yes	Yes
Device	1	1	X	X			Low-pulse			Yes

Table 5: Remote Wakeup Truth Table

6.3 Interrupt Endpoint

The Interrupt Endpoint contains 8 bytes of data and its frame format is defined as: A100_BB00_CCDD_EEFF.

Where BB byte in byte 3:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved				MDINT	FLE	SPLS	PPLS

PPLS: Primarily PHY Link State.
1: Link is up.
0: Link is down.
SPLS: Secondary PHY Link State.
1: Link is up.
0: Link is down.
FLE: Bulk Out Ethernet Frame Length Error.
1: Proprietary Length field has parity error during Bulk Out transaction.
0: Proprietary Length field has no parity error during Bulk Out transaction.
MDINT: Input level of MDINT pin. The MDINT pin can be connected to MDINT# pin of Ethernet Phy.
1: When MDINT input pin = 1.
0: When MDINT input pin = 0.

CCDD byte in byte 5 and 6: Primary Phy's register value, whose offset is given in High byte of EEPROM offset 0Fh.
EEFF byte in byte 7 and 8: Primary Phy's register value, whose offset is given in Low byte of EEPROM offset 0Fh.

7.0 Embedded Ethernet Phy Register Description

Address	Register Name	Description
0h	BMCR	Basic mode control register, basic register.
1h	BMSR	Basic mode status register, basic register.
2h	PHYIDR1	PHY identifier register 1, extended register.
3h	PHYIDR2	PHY identifier register 2, extended register.
4h	ANAR	Auto negotiation advertisement register, extended register.
5h	ANLPAR	Auto negotiation link partner ability register, extended register.
6h	ANER	Auto negotiation expansion register, extended register.
7h	Reserved	Reserved and currently not supported.
8h-Fh	IEEE reserved	IEEE 802.3u reserved.

Table 6: Embedded Ethernet Phy Register Map

7.1 Detailed Register Description

The following abbreviations apply to following sections for detailed register description.

Reset value:

1: Bit set to logic one
0: Bit set to logic zero
X: No set value
Pin#: Value latched from pin # at reset time

Access type:

RO: Read only
RW: Read or write

Attribute:

SC: Self-clearing
PS: Value is permanently set
LL: Latch low
LH: Latch high

7.1.1 Basic Mode Control Register (BMCR)

Address 00h

Bit	Bit Name	Default	Description
15	Reset	0, RW / SC	Reset: 1 = Software reset 0 = Normal operation
14	Loopback	0, RW	Loopback: 1 = Loopback enabled 0 = Normal operation
13	Speed selection	1, RW	Speed selection: 1 = 100 Mb/s 0 = 10 Mb/s
12	Auto-negotiation enable	1, RW	Auto-negotiation enable: 1 = Auto-negotiation enabled. Bits 8 and 13 of this register are ignored when this bit is set. 0 = Auto-negotiation disabled. Bits 8 and 13 of this register determine the link speed and mode.
11	Power down	0, RW	Power down:

			1 = Power down 0 = Normal operation
10	Isolate	(PHYAD = 00000), RW	Isolate: 1 = Isolate 0 = Normal operation
9	Restart auto-negotiation	0, RW / SC	Restart auto-negotiation: 1 = Restart auto-negotiation 0 = Normal operation
8	Duplex mode	1, RW	Duplex mode: 1 = Full duplex operation 0 = Normal operation
7	Collision test	0, RW	Collision test: 1 = Collision test enabled 0 = Normal operation
6:0	Reserved	X, RO	Reserved: Write as 0, read as “don’t care”.

7.1.2 Basic Mode Status Register (BMSR)

Address 01h

Bit	Bit Name	Default	Description
15	100BASE-T4	0, RO / PS	100BASE-T4 capable: 0 = This PHY is not able to perform in 100BASE-T4 mode.
14	100BASE-TX full duplex	1, RO / PS	100BASE-TX full-duplex capable: 1 = This PHY is able to perform in 100BASE-TX full-duplex mode.
13	100BASE-TX half duplex	1, RO / PS	100BASE-TX half-duplex capable: 1 = This PHY is able to perform in 100BASE-TX half-duplex mode.
12	10BASE-T full duplex	1, RO / PS	10BASE-T full-duplex capable: 1 = This PHY is able to perform in 10BASE-T full-duplex mode.
11	10BASE-T half duplex	1, RO / PS	10BASE-T half-duplex capable: 1 = This PHY is able to perform in 10BASE-T half-duplex mode.
10:7	Reserved	0, RO	Reserved: Write as 0, read as “don’t care”.
6	MF preamble suppression	0, RO / PS	Management frame preamble suppression: 0 = This PHY will not accept management frames with preamble suppressed.
5	Auto-negotiation complete	0, RO	Auto-negotiation completion: 1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed
4	Remote fault (Not supported)	0, RO / LH	Remote fault: 1 = Remote fault condition detected (cleared on read or by a chip reset) 0 = No remote fault condition detected
3	Auto-negotiation ability	1, RO / PS	Auto configuration ability: 1 = This PHY is able to perform auto-negotiation.
2	Link status	0, RO / LL	Link status: 1 = Valid link established (100Mb/s or 10Mb/s operation) 0 = Link not established
1	Jabber detect	0, RO / LH	Jabber detection: 1 = Jabber condition detected 0 = No Jabber condition detected
0	Extended capability	1, RO / PS	Extended capability: 1 = Extended register capable 0 = Basic register capable only

7.1.3 PHY Identifier Register 1

Address 02h

Bit	Bit Name	Default	Description
15:0	OUI_MSB	003B hex, RO / PS	OUI most significant bits: Bits 3 to 18 of the OUI are mapped to bits 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored.

7.1.4 PHY Identifier Register 2

Address 03h

Bit	Bit Name	Default	Description
15:10	OUI_LSB	00_0110, RO / PS	OUI least significant bits: Bits 19 to 24 of the OUI are mapped to bits 15 to 10 of this register respectively.
9:4	VNDR_MDL	00_0001, RO / PS	Vendor model number.
3:0	MDL_REV	0001, RO / PS	Model revision number.

7.1.5 Auto Negotiation Advertisement Register (ANAR)

Address 04h

Bit	Bit Name	Default	Description
15	NP	0, RO / PS	Next page indication: 0 = No next page available The PHY does not support the next page function.
14	ACK	0, RO	Acknowledgement: 1 = Link partner ability data reception acknowledged 0 = Not acknowledged
13	RF	0, RW	Remote fault: 1 = Fault condition detected and advertised 0 = No fault detected
12:11	Reserved	X, RW	Reserved: Write as 0, read as “don’t care”.
10	Pause	0, RW	Pause: 1 = Pause operation enabled for full-duplex links 0 = Pause operation not enabled
9	T4	0, RO/PS	100BASE-T4 support: 0 = 100BASE-T4 not supported
8	TX_FD	1, RW	100BASE-TX full-duplex support: 1 = 100BASE-TX full-duplex supported by this device 0 = 100BASE-TX full-duplex not supported by this device
7	TX_HD	1, RW	100BASE-TX half-duplex support: 1 = 100BASE-TX half-duplex supported by this device 0 = 100BASE-TX half-duplex not supported by this device
6	10_FD	1, RW	10BASE-T full-duplex support: 1 = 10BASE-T full-duplex supported by this PHY 0 = 10BASE-T full-duplex not supported by this PHY
5	10_HD	1, RW	10BASE-T half-duplex support: 1 = 10BASE-T half-duplex supported by this PHY 0 = 10BASE-T half-duplex not supported by this PHY
4:0	Selector	0_0001, RW	Protocol selection bits: These bits contain the binary encoded protocol selector supported by this PHY. [0 0001] indicates that this PHY supports IEEE 802.3u CSMA/CD.

7.1.6 Auto Negotiation Link Partner Ability Register (ANLPAR)

Address 05h

Bit	Bit Name	Default	Description
15	NP	0, RO	Next page indication: 1 = Link partner next page enabled 0 = Link partner not next page enabled
14	ACK	0, RO	Acknowledgement: 1 = Link partner ability for reception of data word acknowledged 0 = Not acknowledged
13	RF	0, RO	Remote fault: 1 = Remote fault indicated by link partner 0 = No remote fault indicated by link partner
12:11	Reserved	X, RO	Reserved: Write as 0, read as “don’t care”.
10	Pause	0, RO	Pause: 1 = Pause operation supported by link partner 0 = Pause operation not supported by link partner
9	T4	0, RO	100BASE-T4 support: 1 = 100BASE-T4 supported by link partner 0 = 100BASE-T4 not supported by link partner
8	TX_FD	0, RO	100BASE-TX full-duplex support: 1 = 100BASE-TX full-duplex supported by link partner 0 = 100BASE-TX full-duplex not supported by link partner
7	TX_HD	0, RO	100BASE-TX half-duplex support: 1 = 100BASE-TX half-duplex supported by link partner 0 = 100BASE-TX half-duplex not supported by link partner
6	10_FD	0, RO	10BASE-T full-duplex support: 1 = 10BASE-T full-duplex supported by link partner 0 = 10BASE-T full-duplex not supported by link partner
5	10_HD	0, RO	10BASE-T half-duplex support: 1 = 10BASE-T half-duplex supported by link partner 0 = 10BASE-T half-duplex not supported by link partner
4:0	Selector	0_0000, RO	Protocol selection bits: Link partner’s binary encoded protocol selector.

7.1.7 Auto Negotiation Expansion Register (ANER)

Address 06h

Bit	Bit Name	Default	Description
15:5	Reserved	0, RO	Reserved: Write as 0, read as “don’t care”.
4	PDF	0, RO / LH	Parallel detection fault: 1 = Fault detected via the parallel detection function 0 = No fault detected
3	LP_NP_AB	0, RO	Link partner next page enable: 1 = Link partner next page enabled 0 = Link partner not next page enabled
2	NP_AB	0, RO / PS	PHY next page enable: 0 = PHY not next page enabled
1	Page_RX	0, RO / LH	New page reception: 1 = New page received 0 = New page not received
0	LP_AN_AB	0, RO	Link partner auto-negotiation enable: 1 = Auto-negotiation supported by link partner

8.0 Electrical Specifications

8.1 DC Characteristics

8.1.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDDK	Digital core power supply	- 0.3 to VDDK + 0.3	V
VDD2	Power supply of 2.5V I/O	- 0.3 to VDD2 + 0.3	V
VDD3	Power supply of 3.3V I/O	- 0.5 to VDD3 + 0.5	V
AVDDK	Analog core power supply	- 0.3 to AVDDK + 0.3	V
AVDD3	Power supply of analog I/O	- 0.5 to AVDD3 + 0.5	V
V_{IN2}	Input voltage of 2.5V I/O	- 0.3 to VDD2 + 0.3	V
	Input voltage of 2.5V I/O with 3.3V tolerant	- 0.3 to 3.9	V
V_{IN3}	Input voltage of 3.3V I/O	- 0.3 to VDD3 + 0.3	V
	Input voltage of 3.3V I/O with 5V tolerant	- 0.3 to 5.5	V
T_{STG}	Storage temperature	- 40 to 150	℃

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted in the optional sections of this datasheet. Exposure to absolute maximum rating condition for extended periods may affect device reliability.

8.1.2 Recommended Operating Condition

Symbol	Parameter	Min	Typ	Max	Unit
VDDK	Digital core power supply	2.25	2.5	2.75	V
VDD2	Power supply of 2.5V I/O	2.25	2.5	2.75	V
VDD3	Power supply of 3.3V I/O	3.0	3.3	3.6	V
AVDDK	Analog core power supply	2.25	2.5	2.75	V
AVDD3	Power supply of analog I/O	3.0	3.3	3.6	V
V_{IN2}	Input voltage of 2.5 V I/O	0	2.5	2.75	V
	Input voltage of 2.5 V I/O with 3.3 V tolerance	0	2.5	3.6	V
V_{IN3}	Input voltage of 3.3 V I/O	0	3.3	3.6	V
	Input voltage of 3.3 V I/O with 5 V tolerance	0	3.3	5.25	V
T_j	Commercial junction operating temperature	0	-	115	℃
T_c	Commercial operating temperature	0	-	70	℃

8.1.3 Leakage Current and Capacitance

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IN}	Input current	No pull-up or pull-down	-10	±1	10	μA
I_{OZ}	Tri-state leakage current		-10	±1	10	μA
C_{IN}	Input capacitance		-	3.1	-	pF
C_{OUT}	Output capacitance		-	3.1	-	pF
C_{BID}	Bi-directional buffer capacitance		-	3.1	-	pF

Note: The capacitance listed above does not include pad capacitance and package capacitance. One can estimate pin capacitance by adding a pad capacitance of about 0.5pF and the package capacitance.

8.1.4 DC Characteristics of 2.5V I/O Pins

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VDD2	Power supply of 2.5V I/O		2.25	2.5	2.75	V
Temp	Junction temperature		0	25	115	℃
Vil	Input low voltage	CMOS	-	-	0.7	V
Vih	Input high voltage		1.7	-	-	V
Vt-	Schmitt trigger negative going threshold voltage	CMOS	0.7	1.0	-	V
Vt+	Schmitt trigger positive going threshold voltage		-	1.5	1.7	V
Vol	Output low voltage	|Iol| = 2~16mA	-	-	0.4	V
Voh	Output high voltage	|Ioh| = 2~16mA	1.85	-	-	V
Rpu	Input pull-up resistance		40	75	190	KΩ
Rpd	Input pull-down resistance		40	75	190	KΩ
Iin	Input leakage current	Vin = VDD2 or 0	-10	±1	10	μA
Ioz	Tri-state output leakage current		-10	±1	10	μA

8.1.5 DC Characteristics of 3.3V I/O Pins

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VDD3	Power supply of 3.3V I/O	3.3V I/O	3.0	3.3	3.6	V
Temp	Junction temperature		0	25	115	℃
Vil	Input low voltage	LVTTL	-	-	0.8	V
Vih	Input high voltage		2.0	-	-	V
Vt-	Schmitt trigger negative going threshold voltage	LVTTL	0.8	1.1	-	V
Vt+	Schmitt trigger positive going threshold voltage		-	1.6	2.0	V
Vol	Output low voltage	|Iol| = 2~16mA	-	-	0.4	V
Voh	Output high voltage	|Ioh| = 2~16mA	2.4	-	-	V
Rpu	Input pull-up resistance		40	75	190	KΩ
Rpd	Input pull-down resistance		40	75	190	KΩ
Iin	Input leakage current	Vin = VDD3 or 0	-10	±1	10	μA
Ioz	Tri-state output leakage current		-10	±1	10	μA

8.2 Power Consumption

8.2.1 Internal Phy

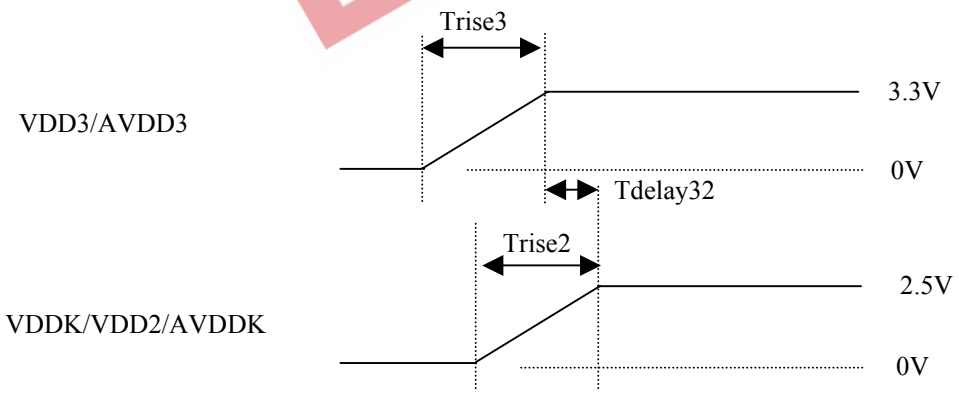
Symbol	Description	Condition	Min	Typ	Max	Units
I_{VDDK2}	Current consumption of VDDK/VDD2, 2.5V	Operating at Ethernet 100Mbps full duplex mode and USB High speed mode	-	25.4	-	mA
I_{VDD3}	Current consumption of VDD3, 3.3V		-	< 1	-	mA
I_{AVDDK}	Current consumption of AVDDK, 2.5V		-	69.3	-	mA
I_{AVDD3}	Current consumption of AVDD3, 3.3V		-	51.1	-	mA
Θ_{JC}	Thermal resistance of junction to case			16.5		°C/W
Θ_{JA}	Thermal resistance of junction to ambient	Still air		46		°C/W

8.2.2 Operating through MII Interface with Internal Ethernet PHY Power-down

Symbol	Description	Condition	Min	Typ	Max	Units
I_{VDDK2}	Current consumption of VDDK/VDD2, 2.5V	Operating in Ethernet 100Mbps full duplex mode through MII interface and in USB High speed mode. The embedded Ethernet PHY is powered down by IPPD bit in Software Reset Register	-	25.4	-	mA
I_{VDD3}	Current consumption of VDD3, 3.3V		-	< 1	-	mA
I_{AVDDK}	Current consumption of AVDDK, 2.5V		-	< 2	-	mA
I_{AVDD3}	Current consumption of AVDD3, 3.3V		-	51.1	-	mA

8.3 Power-up Sequence

At power-up, AX88772 requires the VDD3/AVDD3 power supply to rise to nominal operating voltage within Trise3 and the VDDK/AVDD2/AVDDK power supply to rise to nominal operating voltage within Trise2.

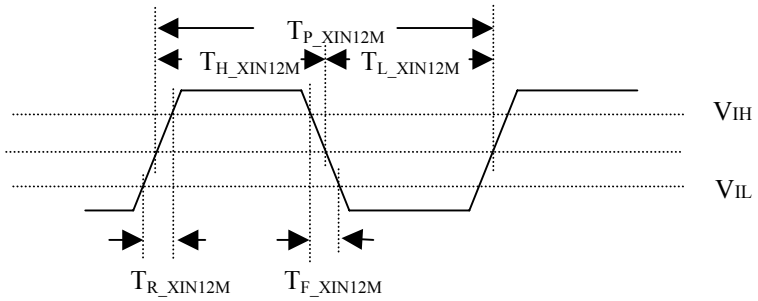


Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{rise3}	3.3V power supply rise time	From 0V to 3.3V	-	-	10	ms
T_{rise2}	2.5V power supply rise time	From 0V to 2.5V	-	-	10	ms
$T_{delay32}$	3.3V rise to 2.5V rise time delay		-5	-	5	ms

8.4 AC Timing Characteristics

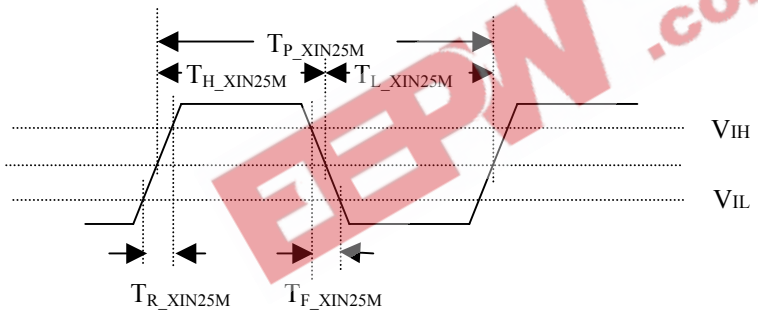
8.4.1 Clock Timing

8.4.1.1 XIN12M



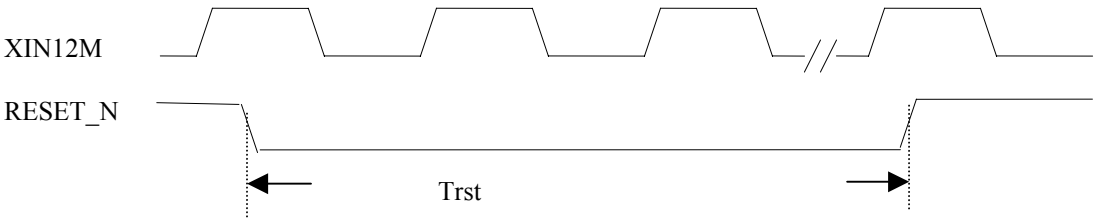
Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{P_XIN12M}	XIN12M clock cycle time		-	83.33	-	ns
T_{H_XIN12M}	XIN12M clock high time		-	41.6	-	ns
T_{L_XIN12M}	XIN12M clock low time		-	41.6	-	ns
T_{R_XIN12M}	XIN12M rise time	V_{IL} (max) to V_{IH} (min)	-	-	1.0	ns
T_{F_XIN12M}	XIN12M fall time	V_{IH} (min) to V_{IL} (max)	-	-	1.0	ns

8.4.1.2 XIN25M



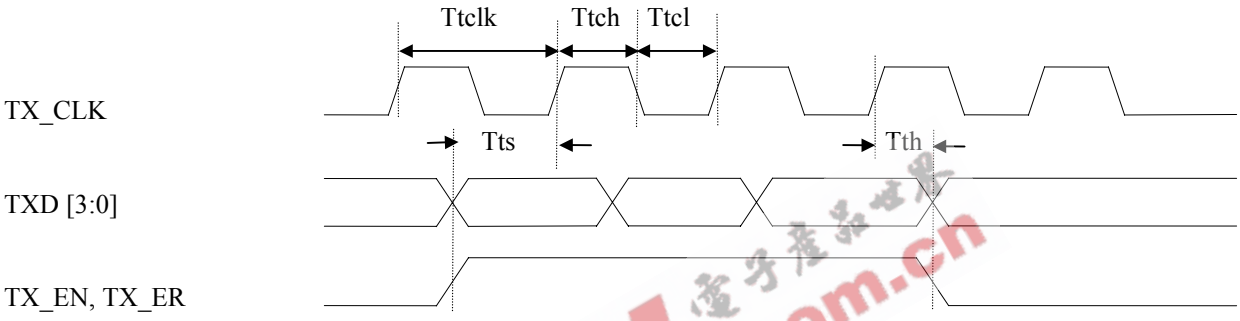
Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{P_XIN25M}	XIN25M clock cycle time		-	40.0	-	ns
T_{H_XIN25M}	XIN25M clock high time		-	20.0	-	ns
T_{L_XIN25M}	XIN25M clock low time		-	20.0	-	ns
T_{R_XIN25M}	XIN25M rise time	V_{IL} (max) to V_{IH} (min)	-	-	1.0	ns
T_{F_XIN25M}	XIN25M fall time	V_{IH} (min) to V_{IL} (max)	-	-	1.0	ns

8.4.2 Reset Timing

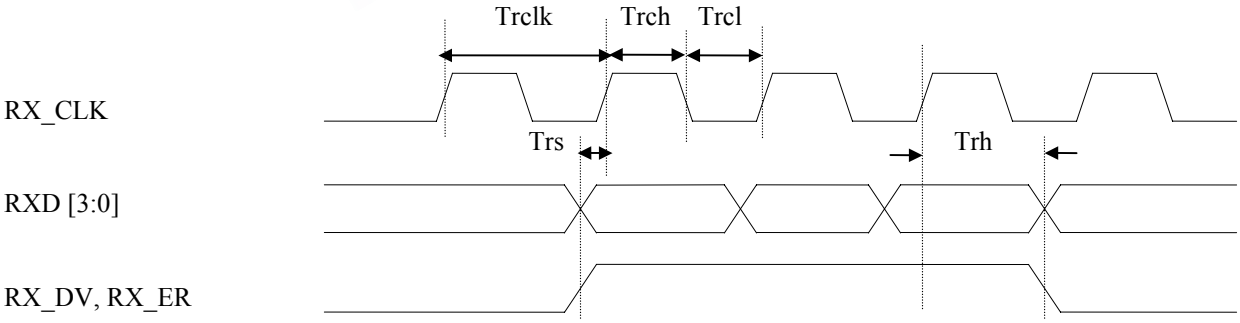


Symbol	Description	Min	Typ	Max	Units
Trst	Reset pulse width (6ms ~10ms) after XIN12M is running	72000	-	-	XIN12M clock cycle

8.4.3 MII Timing (100Mbps)



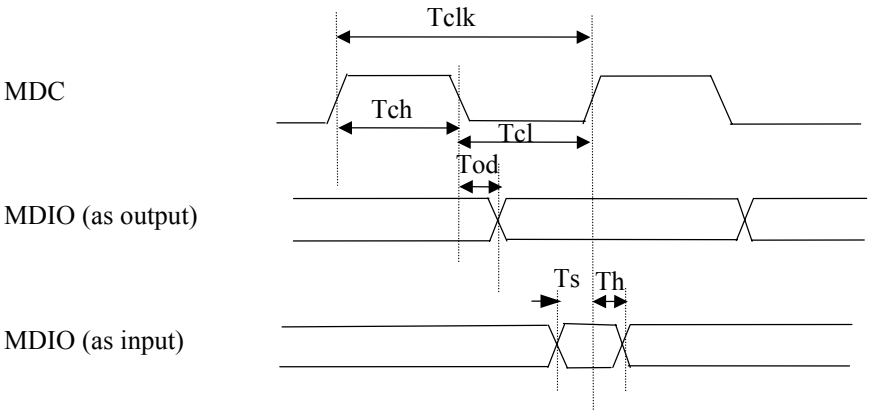
Symbol	Description	Min	Typ	Max	Units
Ttclk	TX_CLK clock cycle time *1	-	40.0	-	ns
Ttch	TX_CLK clock high time *2	-	20.0	-	ns
Ttcl	TX_CLK clock low time *2	-	20.0	-	ns
Tts	TXD [3:0], TX_EN, TX_ER setup time	28.0	-	-	ns
Tth	TXD [3:0], TX_EN, TX_ER hold time	5.0	-	-	ns



Symbol	Description	Min	Typ	Max	Units
Trclk	RX_CLK clock cycle time *1	-	40.0	-	ns
Trch	RX_CLK clock high time *2	-	20.0	-	ns
Trcl	RX_CLK clock low time *2	-	20.0	-	ns
Trs	RXD [3:0], RX_DV, and RX_ER setup time	3.0	-	-	ns
Trh	RXD [3:0], RX_DV, and RX_ER hold time	0.5	-	-	ns

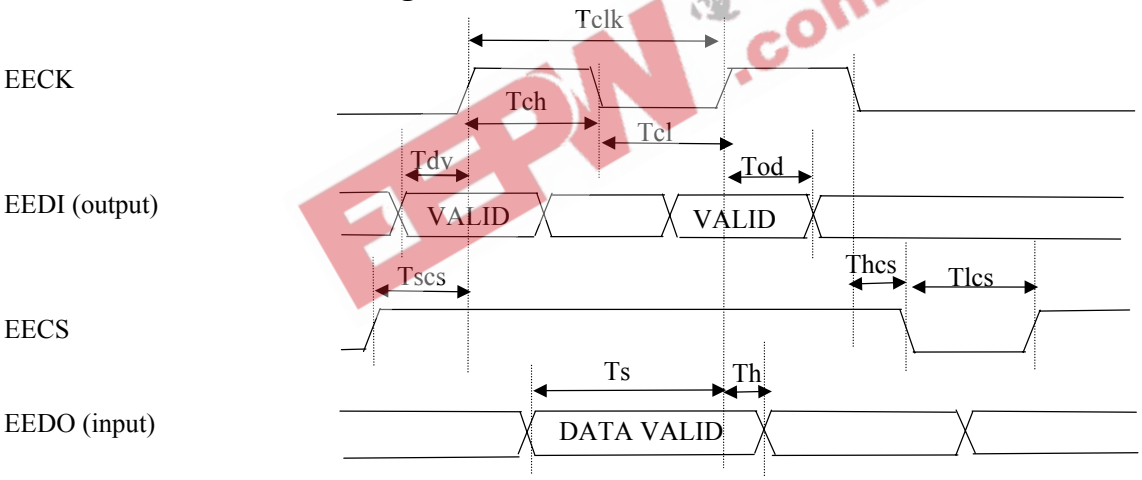
*1: For 10Mbps, the typical value of Ttclk and Trclk shall scale to 400ns.
*2: For 10Mbps, the typical value of Ttch, Ttcl, Trch, and Trcl shall scale to 200ns.

8.4.4 Station Management Timing



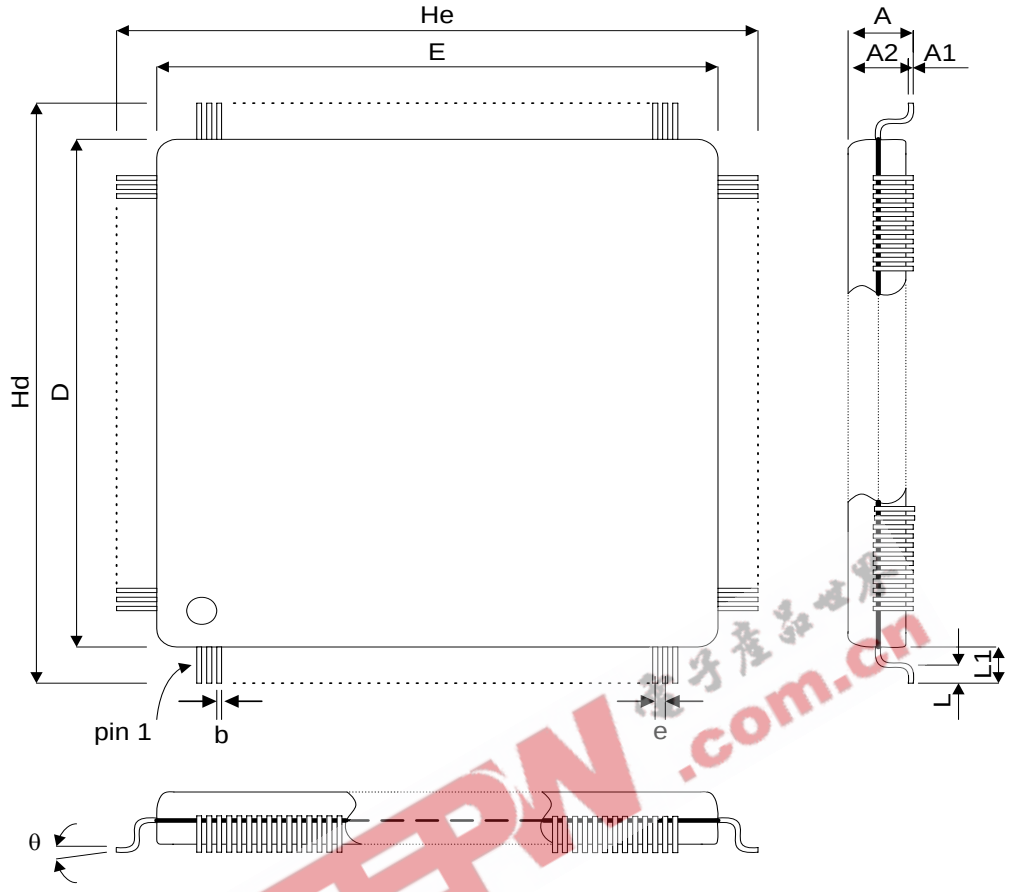
Symbol	Description	Min	Typ	Max	Units
Tclk	MDC clock cycle time	-	666	-	ns
Tch	MDC clock high time	-	333	-	ns
Tcl	MDC clock low time	-	333	-	ns
Tod	MDC clock falling edge to MDIO output delay	0	-	2	ns
Ts	MDIO data input setup time	10	-	-	ns
Th	MDIO data input hold time	0	-	-	ns

8.4.5 Serial EEPROM Timing



Symbol	Description	Min	Typ	Max	Units
Tclk	EECK clock cycle time	-	5333	-	ns
Tch	EECK clock high time	-	2666	-	ns
Tcl	EECK clock low time	-	2666	-	ns
Tdv	EEDI output valid to EECK rising edge time	2666	-	-	ns
Tod	EECK rising edge to EEDI output delay time	2666	-	-	ns
Tscs	EECS output valid to EECK rising edge time	2666	-	-	ns
Thcs	EECK falling edge to EECS invalid time	0	-	-	ns
Tlcs	Minimum EECS low time	23904	-	-	ns
Ts	EEDO input setup time	20	-	-	ns
Th	EEDO input hold time	10	-	-	ns

9.0 Package Information



Symbol	Millimeter		
	Min	Typ	Max
A1	0.05	-	-
A2	1.35	1.40	1.45
A	-	-	1.60
b	0.13	0.18	0.23
D	13.90	14.00	14.10
E	13.90	14.00	14.10
e	-	0.4 BSC	-
Hd	15.85	16.00	16.15
He	15.85	16.00	16.15
L	0.45	0.60	0.75
L1	-	1.00 REF	-
θ	0°	3.5°	7°

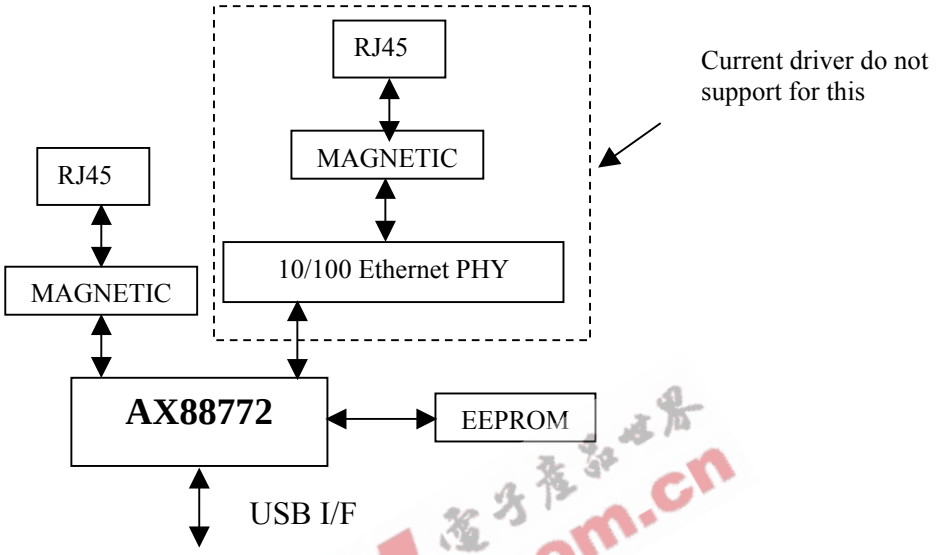
10.0 Ordering Information

AX88772	L	F
Product Name	Package LQFP	Lead Free

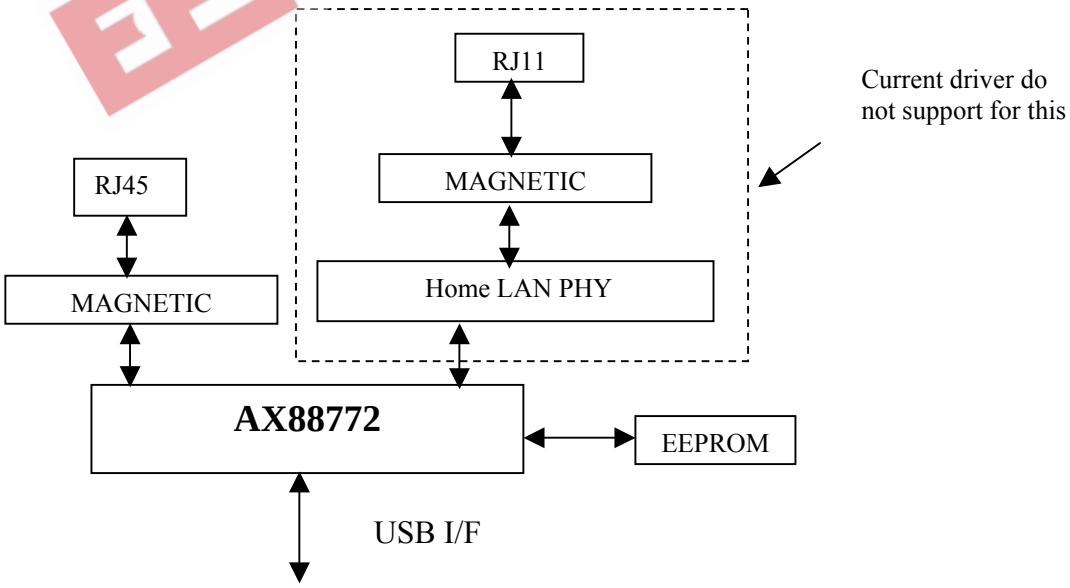
Appendix A: System Applications

Some typical applications for AX88772 are illustrated bellow.

A.1 USB to Fast Ethernet Converter



A.2 USB to Fast Ethernet and/or HomeLAN Combo solution



Revision History

Revision	Date	Comment
V 0.1	1/5/04	Initial Release.
V 0.2	4/16/04	Added power consumption data and updated pin description for pin USB_SPEED_LED.
V 0.3	8/9/04	Changed Bulk In transfer to Endpoint 2 and Bulk Out transfer to Endpoint 3 in section 5.3.
V 0.4	12/23/04	Added thermal data in section 8.2.
V 0.5	1/6/05	Added operating temperature in feature and section 8.1.2.
V 0.6	3/23/05	Added power-up sequence in section 8.3.
V 0.7	6/21/05	Changed the support to 1 USB interface in section 5.2.
V 1.0	9/15/06	1. Added the Power Consumption of MAC to MAC application through MII interface in Section 8.2.2. 2. Correct the EEDO input Setup and Hold time information in Section 8.4.5.
V1.1	4/24/07	1. Added suggested operating frequency range for XIN12M pin in section 2.0. 2. Swaped pin name XIN25M and XOUT25M in section 2.0 and Figure 2. Corrected XIN25M/XOUT25M to 2.5V tolerant pin. 3. Added MII MAC-to-MAC connection diagram in section 3.9. 4. Removed USB V1.0 from datasheet.

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